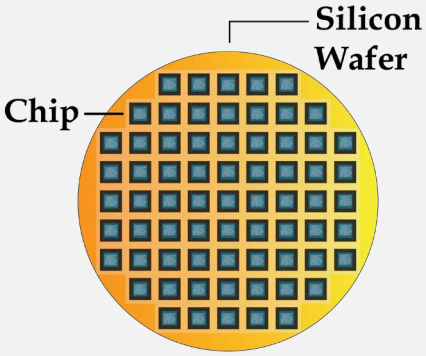
Science & Technology Policy Brief

Semiconductor Chip Manufacturing



Semiconductors or chips power modern electronics and require highly advanced manufacturing processes. This brief outlines the background and technological challenges associated with semiconductor manufacturing.

Summary

- A chip contains millions of electronic switches (transistors) on a flat silicon piece.
- Manufacturing chips involves use of light to print tiny circuits on silicon wafer.
- Three major challenges in manufacturing chips are achieving high resolution, ensuring accuracy and mass production.
- Global supply chain is highly specialised (design, equipment, materials, fabrication) and concentrated in a few places.
- Governments across the world have initiated schemes for domestic chip production facilities.

Background

Semiconductor chips are building blocks of electronic technology.[1] Cars, laptops, smartphones, virtual reality and industrial robots, all rely on chips. The chip industry is a USD 500 billion business that is expected to grow to 1.3 trillion by 2029.[2,3] It is an R&D focussed industry and the global supply chain is highly specialised and concentrated in a few regions. India does not have any high-volume production chip manufacturing facilities (or fabs). The total consumption of electronic chips in India was worth around Rs 1.1 lakh crore in 2020, all of which was met through imports.[4] The central government has announced schemes amounting to Rs 76,000 crore to create fabs in India. This brief outlines various technological challenges associated with chip manufacturing.

Semiconductors are materials which have electrical properties different from conductors (such as copper, aluminium, silver) and insulators (glass, ceramics, plastic). They conduct electricity only under certain conditions. This means that they can be used as switches (ON/OFF) by changing the underlying conditions. A *transistor* is a device made up of a semiconductor that controls electric voltage and current by acting as an ON/OFF switch. This property is utilised to represent states, for instance, OFF as 0 and ON as 1. As all information can be represented as a combination of 0s and 1s (binary system), transistors become fundamental to computing in digital devices.[5]

Modern chips contain millions (and even billions) of transistors and other electronic components in complex three-dimensional circuits (see Figure 1).[6]

The smaller the transistor, the more of these can be packed into the same area. Smaller chips use less electrical energy and generate less heat. Technological advances have helped pack more transistors per chip, doubling every two years, resulting in more computing power. For example, the iPhone 12 (2020) is about a billion times faster than the Apollo 11 guidance computer used in the 1969 US space mission.[7,8] Such compact packing is possible due to reduction in transistor's dimensions to the order of nanometres (nm) which is a billionth of a metre (10^{-9} m). It means a nano-transistor is roughly 50,000-1,00,000 times smaller than the width of a human hair. [9]

The advancement in chip-industry is characterised by process or technology *node numbers*, e.g., 180-nm, 130-nm, and 65-nm. The smaller the node number, the denser the circuitry that results in better performance of the device. [10,11,12,13] For example, advanced smartphones today use 7-nm technology. It means that there are around 10 crore transistors per square mm.[10]

The commonly used semiconductor material is silicon (Si) which is the second most abundant element in earth's crust. Thin circular slices of silicon (called wafers) are used in chip production.

Box 1: Chip node number as per application[14,15,16,17,18]

Chips needed for	Node
Cars	180 nm - 40 nm
Home appliances	130 nm – 90 nm
Laptops, Smartphones	Below 15 nm

Fabrication process: Chips are made up of interconnected complex patterns of transistors created layer by layer on pure silicon wafers (about

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300 mm diameter). The manufacturing of chip involves multiple elements and steps.[19]

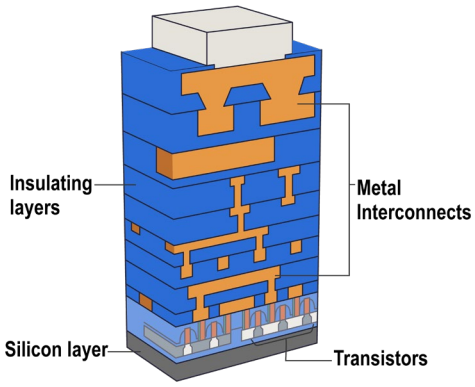
Design: Chips are made up of multiple layers (up to 100) such that patterns are overlayed on top of the previous layer with nanometre precision.[20] Special design software are used to draw a blueprint of 3D architecture of these layers.[21]

Photomask: The blueprint of the designed pattern is then transferred onto an opaque plate with transparent areas, called a 'mask'.[22] The mask is generally four times larger than the intended pattern on the chip.[23] Light passing through this plate imprints the miniaturised version of the pattern on the chip.

Lithography: Lithography or Photolithography is a projection system, i.e., it puts the image of the circuit on to the silicon surface. A silicon wafer is first deposited with layer of silicon or other materials. A thin coating of light-sensitive material is applied on the wafer. Next, the light is projected through the mask and the lens shrinks it and focusses the encoded pattern onto tiny regions of light-sensitive wafer. The exposed patterns are left to bake and develop. Unexposed areas on the photosensitive coating are removed to engrave the pattern onto the surface.

Electrically-charged atoms (ions) are showered on the exposed etched patterns to create transistors. Other materials such as copper wires and silicon dioxide (an insulator) are deposited to connect the transistors in a circuit. The light-sensitive layer is then removed. The lithography and the above process is repeated, and layers with different patterns are created. Finally, layers are stacked up and cut into tiny parts, resulting into a chip.

Figure 1: Inner layers of a chip



Fabrication cleanrooms: Given the small resolution, even a nanoscale particle or virus can potentially damage the pattern on the wafer, and render it useless. A cleanroom (with stable temperature and humidity levels) is required which typically contains 1,000 times fewer dust particles than a sterile operation theatre.[24]

Assembly and testing of chips: Fabrication firms generally make a pizza-sized (~300 mm) wafer printed with many chips. The wafer needs to be cut into actual chips and then encased with a protective layer of ceramic or plastic for easier handling. These 'assembly' or 'packaging' steps are generally done by other companies. A final testing needs to be done to ensure quality. Then, a chip is ready to be plugged in smartphones or laptops.

Technological Challenges

For successful commercial deployment, lithography technologies need to satisfy three criteria: resolution, accuracy and productivity. A machine with higher resolution can make increasingly smaller patterns. A more accurate machine will imprint them without any errors. For mass production, companies need to produce the wafers at a rapid pace. Each of these criteria face several technological challenges.

Challenge 1: Achieving High Resolution

Lithography uses light to expose the patterns on the silicon wafer. The thickness of the patterns cannot be less than the wavelength of light hitting the wafer. Therefore, instead of visible light (wavelength 400-700 nm), deep ultraviolet (DUV) light (wavelength 193 nm) is used.[25]

The amount of light that can be collected and focussed using lenses and mirrors also matters.[26] 193 nm-DUV lithography machines have brought down the resolution to 63 nm from 2,000 nm.[27,28] To go below 63 nm and print even finer details, chipmakers project light through a layer of ultrapure water (or other imaging fluids) between the lens and the silicon wafer.[29] The water increases the amount of light collected and results in improved resolution. Thus, it acts an additional lens. This technique is called DUV *immersion lithography*. A few examples of DUV-made chips are 90, 65 and 45 nm nodes.

However, 193 nm is still larger than the size of patterns that modern chips need. The most advanced chips now use extreme ultraviolet (EUV) light which has about 14 times shorter wavelength than DUV (13.5 nm).[30] EUV effectively acts as a sharper pencil while carving patterns on chips than DUV light. EUV enables the drawing of features up to 10-15 nm. [31,32]

EUV light occurs naturally only in outer space and gets absorbed by air and lenses. Artificial production of EUV light is an extremely difficult task and requires powerful lasers and a sophisticated setup. Special extremely-smooth multi-layered mirrors are required to collect and focus on the wafer during the fabrication.[33] The whole process happens in a vacuum chamber. Globally, ASML in the Netherlands is the only company that makes high-end EUV machines.[25] The latest models of advanced smartphones use EUV-made chips.[34,35] EUV machines are currently only being used by a few top chip manufacturing companies.

Combined DUV and EUV: Since a chip contains many layers stacked on top of each other, the more intricate layers can be printed using EUV and the others with DUV.[23,36] This is done to ensure cost-effectiveness during the chip-making process.

Challenge 2: Ensuring Accuracy

Pattern defects: While EUV light has improved the resolution of lithography systems, making accurate patterns without errors remains a challenge. Currently, EUVs result in random defects on the circuit in the form of imperfectly made holes, line breaks or bridges between two lines.[37] Next-generation EUV machines will need to address this challenge.

Measurement errors: The small wavelength of EUV (13.5 nm) creates problems in measuring the accuracy of the etched patterns.[38] Further reduction in dimensions can impact the quality of accuracy and precision measurement of the patterns.

Semiconductor Production Chain: Company Types[20]

Integrated Device Manufacturers (IDMs): Some companies such as Intel (US) and Samsung Electronics (South Korea) both design and manufacture chips.

Fabrication Companies (Fabs): Fabs manufacture chips under contract for other companies, e.g., Taiwan Semiconductor Manufacturing Company (TSMC), UMC and GlobalFoundries. In 2021, TSMC (54%), Samsung (17%) and GlobalFoundries (7%) constituted about 80% of all manufactured chips.[39] TSMC accounts for more than 90% of advanced chips (below 10 nm nodes).[40]

Fabless Companies: These companies research and design chips but send their production to fabs, e.g. US-based NVIDIA, AMD, and Qualcomm, and MediaTek (Taiwan).

Lithography equipment manufacturers: ASML (Netherlands) and Japan-based Nikon and Canon. In 2020, sales share of all lithography machines (DUVs and EUVs) were: ASML (91%), Nikon (6%) and Canon (3%).[41] Only ASML makes EUV machines used for making advanced chips.

Japan leads the market in speciality chemicals and silicon ingots which are crucial for semiconductor manufacturing.[42]

Challenge 3: Mass Production

Wafer tables and precision printing: The lithography machine first scans and prints on a small portion of the loaded wafer and then moves to the next portion. These steps need to be achieved at a high speed with minimum vibration. Magnetically levitating wafer tables are used in the process.[43,44] Before a pattern is exposed onto a silicon wafer, it must be precisely scanned. While one wafer is being exposed, simultaneously another wafer table measures the positioning of wafer. This is done 20,000 times per second using the machine's sensors with an accuracy of 0.06 nm.

Clean rooms: The area of a typical cleanroom depends on the yield of fabrication plant or fab, i.e., number of wafers produced per month. While the clean room of a mini-fab (~10k wafers per month) is around 30,000 square metres, that of a mega-fab (~25k wafers per month) is 1,00,000 square metres, and of a gigafab (more than 1 lakh wafer per month) is about 1,60,000 square metres.[45,46,47,48] Expensive heating, ventilation and air-conditioning systems are required to maintain the necessary purity levels in such vast spaces.

High purity water: Presence of even a nano-sized particle (chemical impurities, bacteria or virus) in the water used for immersion lithography can sabotage the intricate design on the wafer.[49,50] Also, since the set up is moving at high-speed, water bubbles should not form; otherwise, the resolution of the equipment will be affected. Therefore, dissolved gases are removed from water before it is put into the system.

During lithography, various unwanted particles, chemicals and metal debris (from construction of connections between transistors) are left. A sequential wet cleaning using ultrapure water is needed to rinse off the contamination. Also, more layers in a chip increase the amount of water needed.

Waste water treatment: More than 400 chemical products are typically used in a chip production plant.[51] The waste water left over from the wet cleaning steps contains high amounts of chemicals. Exposure to these chemicals can potentially cause health problems. Hence, proper water treatment is critical.[51,52] Big fabrication companies such as TSMC (Taiwan) recycle about 87% of the waste water whereas the industry average is 42%.[53,54]

Timeline of technological milestones

1947/1948: First Transistor[55]
1959: Integrated circuit (IC) or Chip[56]
1970: First commercial memory chip (DRAM)[57]
1971: First commercial microprocessor/CPU (10 micrometre (µm or 10^{-6} m) nodes, ~2300 transistors)[58]
2001: Intel Pentium 4 chip (180 nm, ~42 million transistors)[58]
2004/2005: DUV immersion Lithography[25,59], 65-nm process node
2019: First commercial EUV-made 7-nm chip[60,61]
2022: Apple M1 Ultra (~114 billion transistors) chip[62]

Size and Cost of Lithography Machines: The smaller the patterns on the chip, the bigger the lithography machine needed, as a larger set of lens or mirrors are required and more energy-intensive equipment is needed. The current EUV machines are the size of a school bus and contain one lakh moving parts.[63] The cost of a basic EUV machine is about USD 150 million.[64] The next generation EUV machine is even bigger than the basic version and costs about USD 300 million.[65]

In contrast, DUV immersion systems are smaller and cost around 60 million euros. The price of dry

systems (without water or imaging fluids between lens and wafer) averages around 20 million euros.[66]

Looking Ahead

Next-generation EUV machines: It took almost 30 years to build an EUV light source with 13.5 nm. The next-generation EUV machines rely on increasing the amount of light which the mirrors can collect. These systems with larger mirrors are expected to enter the market by 2025 or 2026. They would reduce the minimum feasible resolution on the circuit from 13 nm to 8 nm.[31, 67]

Increasing performance: As the resolution size starts hitting limits, other methods for increasing computing power will have to be used.[38] These will involve stacking transistors on top of each other, tweaking with their structure, and improving the interconnects between transistors.

Quantum effects: The smallest transistors usually suffer from quantum effects, e.g., getting unwanted leakage current even when transistor is in off state.[38] These effects will become more pronounced as pattern gets smaller and smaller. Such effects can interfere and disrupt the operation of the chip.

Power and cooling problem: As the dimensions of transistors are reduced, it becomes difficult to bring power into the chip.[38] Extracting heat from the chip is also a problem. Improved and efficient power delivery and cooling mechanisms are needed to advance further.

Indian Semiconductor Scenario

At present, India does not have any commercial fab, and all chip requirement is met through imports. However, various multinationals as well as Indian IC design service providers have large design houses in India.[42,68] Once the designs are completed, they are sent for fabrication to United States, South Korea or Taiwan.

R&D in Semiconductors in India: The Center of Excellence in Nanoelectronics launched in 2006 have developed R&D expertise in India. Ministry of Electronics and Information Technology (MeitY) Special Manpower Development Program (SMDP) has enabled IC design R&D and talent development.[69,70] Semi-Conductor Lab (SCL) Mohali's 180nm CMOS line has been leveraged by strategic agencies like ISRO, DRDO, and academic institutions to develop design and technology IP as well as talent development. To address the lack of domestic chip manufacturing capabilities, India has initiated different programs that are listed below.

Semicon India Program: With a total outlay of Rs 76,000 crore (~ USD 10 billion), India has approved three major schemes to address the issues related to semiconductor industry.[71]

(i) *Semiconductor fabs*: Fiscal support of 50% of the total project cost will be provided for construction of two new fabrication facilities.[72]

(ii) *Other chip-related fabs and assembly and testing facilities:* Fiscal support of 50% for setting up compound semiconductors/ light-based silicon semiconductors/sensors fabs. Compound semiconductors refer to chips made up of two elements, e.g., Gallium Nitride (GaN) as opposed to pure silicon. Similar support is also given for the construction of assembly, testing, marking and packaging (ATMP) facilities and Outsourced Semiconductor Assembly and Test (OSAT) companies.[73]

Government Support in US and EU:

US CHIPS Act: The Creating Helpful Incentives to Produce Semiconductors and Science (CHIPS) Act of 2022, allocated around USD 280 billion to boost semiconductor capacity, accelerate innovation and create a bigger STEM workforce over a period of 10 years.[74] About USD 200 billion is given for R&D and commercialisation followed by constructing domestic chip manufacturing facilities (~USD 53 billion).

EU Chips Act: The Act aims to increase to the chip production in EU from less than 10% to 20% of total world production. EU has mobilised about USD 46 billion of public and private investment until 2030 to attain the manufacturing goal.[75]

(iii) *Design-Linked Scheme:* This scheme provides financial incentives and infrastructure support for development of electronic design components such as IC, chipsets and new chip architectures over a period of five years.

The program also includes the construction of display (e.g., LCD screens) fabs and modernisation of SCL Mohali. India Semiconductor Mission (ISM) is the nodal agency for the implementation of schemes for the development of chips and manufacturing ecosystem in India.

Scheme for Promotion of Manufacturing of Electronic Components and Semiconductors (SPECS): MeitY has an additional scheme which provides financial incentive of 25% on capital expenditure for domestic manufacturing of electronic components, construction of semiconductors fab units and ATMP units.[76]

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